Sughrue
SUGHRUE MION, PLLC

2100 Pennsylvania Avenue, NW
Washington, DC 20037-3213
T 202.293.7060
F 202.293.7860

www.sughrue.com

FAX

Date	July 8, 2003		
To	Examiner Minh T. NGUYEN		
Of	PTO Group Art Unit 2816		
Fax	(703) 872-9319 (After Final Fax No. for Art Group 2800)		
From	Jason Beckstead (Reg. No. 48,232)		
Subject	Re-submission of Amendment Originally Filed 6-24-03		
Our Ref	Q65962	Appln No	09/940,472
Conf No	4891	Inventors	Katsuji KIMURA
Pages	10 (including cover sheet)		

FAX RECEIVED
JUL 0 8 2003
TECHNOLOGY CENTER 2800

Please call attention to problems with this transmission by return fax or telephone. Thank you.

This fax filing includes:
1. This cover sheet
2. Filing Receipt Showing OIPE Stamp of 6-24-03 for a (1) Second Amendment under 1.116 and (2) Ext. of Time for Same
3. Aforementioned Second Amendment Filed 6-24-03 and Ext. of Time Filed 6-24-03

CERTIFICATION OF FACSIMILE TRANSMISSION

Sir:

I hereby certify that the above identified correspondence is being facsimile transmitted to Examiner Minh T. NGUYEN, C/O Art Group 2800, at the Patent and Trademark Office on July 8, 2003 at (703) 872-9319.

Respectfully submitted,

Jason C. Beckstead
Reg. No. 48,232

77

FILING RECEIPT
PLEASE DATE STAMP AND RETURN TO US - BOX 235X

In re application of

Katsuji KIMURA

Appln. No.: 09/940,472

Confirmation No.: 4891

Filed: August 29, 2001

Group Art Unit: 2816

Examiner: Minh T. NGUYEN

For: LINEAR VOLTAGE SUBTRACTOR/ADDER CIRCUIT AND MOS DIFFERENTIAL AMPLIFIER CIRCUIT THEREFOR

PAPER(S) FILED ENTITLED:

1. **Second Amendment Under 37 C.F.R. §1.116**
2. **Petition for Extension of Time** (in duplicate with Check No. *224790* in the amount of *$300.00*).

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE

23373
PATENT TRADEMARK OFFICE

DOCKET NO.: Q65962
ATTORNEY/SEC: HLB/JCB/clf
Date Filed: June 24, 2003

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Katsuji KIMURA

Docket No: Q65962

Appln. No.: 09/940,472

Group Art Unit: 2816

Confirmation No.: 4891

Examiner: Minh T. NGUYEN

Filed: August 29, 2001

For: LINEAR VOLTAGE SUBTRACTOR/ADDER CIRCUIT AND MOS DIFFERENTIAL AMPLIFIER CIRCUIT THEREFOR

PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

JUL 2 2003

Sir:

Pursuant to 37 C.F.R. § 1.136, Applicant hereby petitions for an extension of time of two months, extending the time for responding to the Office Action of January 27, 2003, to June 27, 2003.

A check for the statutory fee of $300.00 is attached ($410.00 less $110.00, which was previously paid on May 16, 2003, for a one-month extension of time). The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Jason C. Beckstead

Jason C. Beckstead
Registration No. 48,232

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE

23373

PATENT TRADEMARK OFFICE

Date: June 24, 2003

SECOND AMENDMENT UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE
GROUP 2816
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Katsuji KIMURA

Appln. No.: 09/940,472

Confirmation No.: 4891

Filed: August 29, 2001

Docket No: Q65962

Group Art Unit: 2816

Examiner: Minh T. NGUYEN

For: LINEAR VOLTAGE SUBTRACTOR/ADDER CIRCUIT AND MOS DIFFERENTIAL AMPLIFIER CIRCUIT THEREFOR

SECOND AMENDMENT UNDER 37 C.F.R. § 1.116

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In further response to the Office Action dated January 27, 2003, and supplementing the Amendment Under 37 C.F.R. § 1.116 filed May 16, 2003, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please replace the formula at the top of page 21 with the following as a typographical error has been detected:

$$V_S = \frac{V_1 + V_2}{2} - \sqrt{\frac{I_o}{2\beta}} - Vth \qquad (25)$$

Please add the following immediately after formula (25) on page 21:

This is equivalent to the notation: $V_s=(V_1+V_2)/2 - \sqrt{[I_0/(2\beta)]} - V_{TH}$, and shows that the common source voltage Vs includes a constant offset voltage:

$$-\sqrt{[I_0/(2\beta)]}-V_{TH}.$$

Second Amendment Under 37 C.F.R. § 1.116
U.S. Application No. 09/940,472

Attorney Docket No. Q65962

REMARKS

Claims 1 - 4 are presently pending in the application. A reply under 37 C.F.R. § 1.116 was previously filed on May 16, 2003. In response to this reply, the Examiner mailed an Advisory Action on May 27, 2003, informing the Applicant that the rejections would stand as the Examiner believed the grounds of rejection to be proper.

On June 9, 2003, the Applicant's representative called the Examiner to discuss the rejection. During this discussion the Examiner noted the intricacy of the functional language of claims 1 and 3. It is upon this functional language, that stems from the structure of the instant invention as claimed, that Applicant respectfully requests further consideration.

Specifically, the prior art cited in the grounds of rejection fails to possess the structure and function of an adder circuit as claimed in independent claims 1 and 3. That is, U.S.P. No. 5,602,509 ("Kimura") discloses transistors M51, M52, M53 and M54 connected as a squaring circuit. This circuit arrangement prevents the Kimura reference from operating as an adder.

In other words, the aforementioned transistors and general arrangement of the Kimura reference prevents the Kimura reference from possessing a linear addition function at the common source of transistors M56 and M57 (node B) as required by independent claims 1 and 3 of the instant invention. Simply stated, the circuit of Kimura does not provide a linear addition output voltage $(V_1+V_2)/2$ as is required to anticipate the adder circuit claimed in this application.

Second Amendment Under 37 C.F.R. § 1.116
U.S. Application No. 09/940,472

Attorney Docket No. Q65962

I. Rejection Under 35 U.S.C. § 102(b)

Claims 1 - 4 stand rejected as allegedly being anticipated by U.S.P. No. 5,602,509 ("Kimura"). For the following reasons, this rejection is respectfully traversed.

Independent Claims 1 and 3

Independent claims 1 and 3 recite (among other things) a voltage adder circuit wherein the addition function derives at commonly coupled source electrodes of first and second MOS transistors. It is asserted that the prior art relied upon in the grounds of rejection (U.S.P. No. 5,602,509 ("Kimura")) fails to teach or suggest at least these elements of the independent claims.

The grounds of rejection compare the source electrodes of transistors M56 and M57 (coupled at node B in Figure 1) to the commonly coupled source electrodes of the instant invention. In response, it is respectfully averred that Kimura is not an adder circuit and cannot meet the limitations of the instant invention, as explained below.

In Fig. 1 of Kimura, transistors M51 - M54 constitute a squaring circuit. The circuit of Kimura operates linearly when $n=1+2/\sqrt{3}$ (=2.1547). That is, the following relation should be satisfied:

$$I_{DS6}+I_{DS7}=I_0+(1/2)\beta Vi^2 \quad (1)$$

where I_0 is a constant current.

By applying the current rule of Kirchhoff's law at node B, the following equation is obtained:

$$I_{DS6}+I_{DS7}+I_{DS5}=aI \quad (2)$$

By substituting formula (1) for formula (2), the following formula is obtained:

$$I_{DS5}=aI-I_0-(1/2)\beta\, Vi^2 \qquad (3)$$

where aI is greater than or equal to $I_0+(1/2)\beta\, Vi^2$.

Drain current I_{DS5} of transistor M55 is represented as follows:

$$I_{DS5}=\beta\,(V_A - V_B - V_{TH})^2 \qquad (4)$$

From formulae (3) and (4), the following relation is obtained:

$$V_A - V_B - V_{TH}= \sqrt{[(1/\beta)(aI - I_o)-(1/2)Vi^2]} \qquad (5)$$

Therefore, by substituting formula (6), i.e.:

$$V_B=(V_1+V_2)/2 - \sqrt{[I_o/(2\beta)]} - V_{TH} \qquad (6)$$

for formula (5), the following relation is obtained:

$$V_A = (V_1+V_2)/2 - \sqrt{[I_o/(2\beta)]} + \sqrt{[(1/\beta)(aI - I_O)-(1/2)Vi^2]} \qquad (7)$$

From formula (7), it is readily apparent that in the circuit of Fig. 1 of Kimura, the voltage of node A also includes a component: $\sqrt{[(1/\beta)(aI - I_o)-(1/2)Vi^2]}$ which varies depending on the differential input voltage.

Therefore, because the voltage at node A varies depending upon the differential input voltage, and due to the relationship between node A and node B, the circuit of Kimura fails to operate as an adder circuit. Simply stated, the circuit of Kimura does not provide a linear addition output voltage $(V_1+V_2)/2$ as is required to anticipate the function of an adder circuit as in the instant invention.

Second Amendment Under 37 C.F.R. § 1.116
U.S. Application No. 09/940,472

Attorney Docket No. Q65962

In light of the previous, it is averred that independent claims 1 and 3 recite features that are entirely absent in the prior art relied upon in the grounds of rejection. Accordingly, the Examiner is respectfully requested to reconsider and withdraw this anticipation rejection.

Dependent Claims 2 and 4

Dependent claims 2 and 4 are averred to be patentable at least by virtue of their dependence upon their respective base claims, in addition to their individual recitations.

II. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

Jason C. Beckstead

Jason C. Beckstead
Registration No. 48,232

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
PATENT TRADEMARK OFFICE

Date: June 24, 2003

Second Amendment Under 37 C.F.R. § 1.116
U.S. Application No. 09/940,472

Attorney Docket No. Q65962

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification is changed as follows:

The formula at the top of page 21 is changed as noted below (please note that a "2" ("two") is added next to the "beta" symbol):

$$V_S = \frac{V_1 + V_2}{2} - \sqrt{\frac{I_o}{2\beta}} - V_{th} \qquad (25)$$

The following is added immediately after formula (25) on page 21:

This is equivalent to the notation: $V_S=(V_1+V_2)/2 - \sqrt{[I_0/(2\beta)]} - V_{TH}$, and shows that the common source voltage Vs includes a constant offset voltage:

$$-\sqrt{[I_0/(2\beta)]}-V_{TH}.$$